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EXAMINER	
NGUYEN, TOAN D	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/909,896	AGAZZI ET AL.
	Examiner	Art Unit
	Toan D. Nguyen	2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-51 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 1 line 11, the limitation "1/s, where s is an integer greater than one". No support for this feature could be found in the original specification. Similar problems exist in claim 9 line 8, and claim 18 line 10.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azadet et al. (EP 1006697) in view of Winter et al. (Electrical Signal Processing Techniques In Long-Haul, Fiber-Optic Systems, AT&T Bell Laboratories).

As far as understood with respect to claim 1, Azadet et al. disclose parallel signal processing for equalization on fibre channels, comprising the steps of:

3) generating N sampling signals having a first frequency that is lower than the symbol rate (page 2 lines 30-35), the N sampling signals shifted in phase relative to one another where N is an integer greater than one (figure 2, page 3 lines 19-20, lines 25-27 and figure 3, page 3 lines 32-36);

4) controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases, so as to produce samples (figure 3, page 3 lines 37-38);

5) performing at least one M-path parallel digital process on the samples, wherein M=kN and k is one of an integer greater than one and 1/s, where s is an integer greater than one (page 3 lines 19-20, and page 3 line 57 to page 4 line 7); and

6) generating a digital signal representation of the data signal from the samples (page 3 line 57 to page 4 line 7).

Azadet et al. disclose an electrical signal having a symbol rate (figure 1, page 3 lines 23-25). However, Azadet et al. do not expressly disclose:

1) receiving an optical data signals;

2) converting the optical data signal to an electrical signal. In an analogous art, Winter et al disclose:

1) receiving an optical data signals (figure 1, page 305.3.1, col. 2 line 12);

2) converting the optical signal to an electrical signal (page 305.3.1, col. 2 lines12-13 and page 305.3.2, col. 1 lines 6-7).

One skilled in the art would have recognized receiving an optical data signals to use the teachings of Winter et al in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the receiving an optical data signals as taught by Winter et al. in Azadet et al.'s system with the motivation being to mitigate the effect of intersymbol interference in long-haul, fiber-optic systems (Abstract lines 1-3).

For claim 2, Azadet et al. disclose wherein step (5) comprises performing an equalization process on the samples (figure 4, reference 500, page 3 lines 57-58).

For claim 3, Azadet et al. disclose wherein step (5) further comprises the step of performing Viterbi equalization (figure 6, reference 650) on the digital electrical signal (page 4 line 2).

For claim 4, Azadet et al. disclose wherein step (5) further comprises performing a feed-forward equalization process on the samples (figure 5, reference 510) (page 4 line 16).

For claim 5, Azadet et al. disclose wherein step (5) further comprises performing a decision feedback equalization process on the samples (page 4, line 20).

For claim 6, Azadet et al. disclose wherein step (5) further comprises performing Viterbi equalization (figure 6, reference 650) and feed-forward equalization process (figure 5, reference 510) on the samples (page 2, lines 40-42).

For claim 7, Azadet et al. disclose wherein step (5) further comprises performing Viterbi equalization (figure 6, reference 650) and decision feedback equalization processes on the samples (page 2, lines 40-42).

For claim 8, Azadet et al. disclose wherein step (5) further comprises performing one or more of the following types of equalization processes on the samples:

Viterbi equalization (figure 6, reference 650);

feed-forward equalization (figure 5, reference 510); and

decision feedback equalization (page 2, lines 40-42).

As far as understood with respect to claim 9, Azadet et al. disclose parallel signal processing for equalization on fibre channels, comprising the steps of:

an analog-to-digital converter ("ADC") array of N ADC paths, wherein N is an integer greater than 1, each ADC path including an ADC path input (figure 1, reference 130) coupled to an output of the optical-to electrical converter (page 3 lines 27-28); and

an M-path digital signal processor (figure 1, reference 140) coupled to the ADC array, where M=kN and k is one of an integer greater than one and 1/s, where s is an integer greater than one (figure 1, reference 130) (page 3 lines 19-20 and lines 27-29).

However, Azadet et al. do not expressly disclose:

a receiver input;

an optical-to-electrical converter coupled to the receive input. In an analogous art, Winter et al. disclose: a receive input (figure 1, page 305.3.1, col. 2 line 12); an optical-to-electrical converter coupled to the receive input (page 305.3.1, col. 2 lines 12-13 and page 305.3.2, col. 1 lines 6-7).

One skilled in the art would have recognized an input to use the teachings of Winter et al in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the input as taught by Winter et al. in Azadet et al.'s system with the motivation being to mitigate the effect of intersymbol interference in long-haul, fiber-optic systems (Abstract lines 1-3).

For claim 10, Azadet et al. disclose wherein the digital signal processor includes an equalizer (figure 4, reference 500, page 3 lines 57-58).

For claim 11, Azadet et al. disclose wherein the equalizer comprises a Viterbi equalizer (figure 6, reference 650) (page 4 lines 1-2).

For claim 12, Azadet et al. disclose the equalizer comprises a feed forward equalizer (figure 5, reference 510) (page 4 line 16).

For claim 13, Azadet et al. disclose the equalizer comprises a decision feedback equalizer (page 4, line 20).

For claim 14, Azadet et al. disclose wherein the equalizer comprises a Viterbi equalizer (figure 6, reference 650) and a feed-forward equalizer (figure 5, reference 510) (page 2 lines 40-42).

For claim 15, Azadet et al. disclose wherein the equalizer comprises a Viterbi equalizer (figure 6, reference 650) and a decision feedback equalizer (page 2, lines 40-42).

For claim 16, Azadet et al. disclose wherein the equalizer comprises a feed-forward equalizer (figure 5, reference 510) and a decision feedback equalizer (page 2, lines 40-42).

For claim 17, Azadet et al. disclose wherein the equalizer comprises one or more of the following types of equalization on the digital electric signal:

a Viterbi equalizer (figure 6, reference 650);

a feed-forward equalizer (figure 5, reference 510); and

a decision feedback equalizer (page 2, lines 40-42).

As far as understood with respect to claim 18, Azadet et al. disclose parallel signal processing for equalization on fibre channels, comprising the steps of:

means for generating N sampling signals having a first frequency that is lower than the symbol rate (page 2 lines 30-35), the N sampling signals shifted in phase relative to one another (figure 2, page 3, lines 25-27 and figure 3, page 3 lines 32-36);

means for controlling N analog-to-digital converter ("ADC") paths with the N sampling signals to sample the electrical signal at the phases, so as to produce samples (figure 3, page 3 lines 37-38);

means for performing at least one M-path parallel digital process on the samples, wherein M=kN and k is one of an integer greater than one and 1/s, where s is an integer greater than one (page 3 lines 19-20, and page 3 line 57 to page 4 line 7); and

means for generating a digital signal representation of the data signal from the samples (page 3 line 57 to page 4 line 7).

Azadet et al. disclose an electrical signal having a symbol rate (figure 1, page 3 lines 23-25). However, Azadet et al. do not expressly disclose:

means for receiving an optical data signals;

means for converting the optical data signal to an electrical signal.

In an analogous art, Winter et al. disclose:

means receiving an optical data signals (figure 1, page 305.3.1, col. 2 line 12);

means for converting the optical data signal to an electrical signal (page 305.3.1, col. 2 lines12-13, and page 305.3.2, col.1 lines 6-7).

One skilled in the art would have recognized means for receiving an optical data signals to use the teachings of Winter et al. in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the means for receiving an optical data signals as taught by Winter et al. in Azadet et al.'s system with the motivation being to mitigate the effect of intersymbol interference in long-haul, fiber-optic systems (Abstract lines 1-3).

For claim 19, Azadet et al. disclose wherein the means for performing digital processes on the samples include means for equalizing the digital electrical signal (figure 4, reference 500, page 3 lines 57-58).

For claim 20, Azadet et al. disclose wherein the means for equalizing samples comprise means for performing Viterbi equalization process (figure 6, reference 650) on the samples (page 4 line 2).

For claim 21, Azadet et al. disclose wherein the means for equalizing the samples comprise means for performing a feed-forward equalization process (figure 5, reference 510) on the samples (page 4 line 16).

For claim 22, Azadet et al. disclose wherein the means for equalizing the samples comprise means for performing decision feedback equalization process on the samples (page 4, line 20).

For claim 23, Azadet et al. disclose wherein the means for equalizing the samples comprise means for performing Viterbi equalization (figure 6, reference 650) and feed-forward equalization processes on the samples (figure 5, reference 510) (page 2 lines 40-42).

For claim 24, Azadet et al. disclose wherein the means for equalizing the samples comprise means for performing Viterbi equalization (figure 6, reference 650) and decision feedback equalization processes on the samples (page 2, lines 40-42).

For claim 25, Azadet et al. disclose wherein step (1) comprises receiving the optical data signal from a multimode optical fiber (Abstract, page 1 col. 2 lines 1-4) and

step (5) comprises equalizing multimode dispersion from the multimode optical fiber (Abstract).

For claims 26-30, Azadet et al. do not expressly disclose wherein step (1) comprises receiving the optical data signal from a single mode optical fiber and step (5) comprises equalizing chromatic and/or waveguide dispersion from the single mode optical fiber. In an analogous art, Winter et al. disclose wherein step (1) comprises receiving the optical data signal from a single mode optical fiber (figure 1, page 305.3.1, col. 2 line 12) and step (5) comprises equalizing chromatic and/or waveguide dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29).

Azadet et al. disclose wherein step (1) comprises receiving the optical data signal from a multimode optical fiber (figure 3, col. 3 lines 32-58), and Winter et al. in view of Azadet et al. disclose step (5) comprises equalizing chromatic and/or waveguide dispersion from the multimode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29 as set forth in claim 27); wherein step (1) comprises receiving the optical data signal from a single mode optical fiber (figure 1, page 305.3.1 col. 2 line 12) and step (5) comprises equalizing polarization mode dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 2 lines 28-31 as set forth in claim 28); wherein step (1) comprises receiving the optical data signal from a single mode optical fiber (figure 1, page 305.3.1 col. 2 line 12) and step (5) comprises equalizing dispersion induced in the single mode optical fiber by laser chirping (page 305.3.2, col. 2 lines 10-14 as set forth in claim 29); wherein step (1) comprises receiving the optical data signal from a transmitter that lacks external modulators (figure 1, page 305.3.1, col. 2 lines 3-5 and col. 2 line 12) and step

(5) comprises equalizing excess dispersion induced by laser chirping (page 305.3.2; col. 2 lines 10-14 as set forth in claim 30).

One skilled in the art would have recognized receiving the optical data signal from a single mode optical fiber to use the teachings of Winter et al. in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use receiving the optical data signal from a single mode optical fiber as taught by Winter et al. in Azadet et al.'s system with the motivation being to convert the optical signal, $s_0(t)$, to an electrical signal (page 305.3.1 lines 12-14).

For claim 31, Azadet et al. disclose wherein the input is coupled to a multimode optical fiber and the equalizer equalizes multimode dispersion from the multimode optical fiber (Abstract).

For claims 32-36, Azadet et al. do not expressly disclose wherein the input is coupled to a single mode optical fiber and said equalizer equalizes chromatic and/or waveguide dispersion from the single mode optical fiber. In an analogous art, Winter et al disclose wherein said input is coupled to a single mode optical fiber (figure 1, page 305.3.1, col. 2 line 12) and said equalizer equalizes chromatic and/or waveguide dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29). Azadet et al. disclose wherein the input is coupled to a multimode optical fiber (figure 3, col. 3 lines 32-58) and Winter et al in view of Azadet et al disclose the equalizer equalizes chromatic and/or waveguide dispersion from the multimode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29 as set forth in claim 33); Azadet et al. disclose wherein the input is coupled to a multimode optical fiber (figure 3, col. 3 lines 32-58) and

Winter et al. in view of Azadet et al. disclose the equalizer equalizes polarization mode dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 2 lines 28-31 as set forth in claim 34); wherein the input is coupled to a single mode optical fiber (figure 1, page 305.3.1, col. 2 line 12) and the equalizer equalizes dispersion induced in the single mode optical fiber by laser chirping (page 305.3.2, col. 2 lines 10-14 as set forth in claim 35); wherein the input receives the optical data signal from a transmitter that lacks external modulators (figure 1, page 305.3.1, col. 2 lines 3-5 and col. 2 line 12) and the equalizer equalizes excess dispersion induced by laser chirping (page 305.3.2, col. 2 lines 10-14 as set forth in claim 36).

One skilled in the art would have recognized the input is coupled to a single mode optical fiber and said equalizer equalizes chromatic and/or waveguide dispersion from the single mode optical fiber to use the teachings of Winter et al. in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the input is coupled to a single mode optical fiber and said equalizer equalizes chromatic and/or waveguide dispersion from the single mode optical fiber as taught by Winter et al. in Azadet et al.'s system with the motivation being to convert the optical signal, $s_0(t)$, to an electrical signal (figure 1, page 305.3.1 lines 12-14).

For claim 37, Azadet et al. disclose wherein the means for receiving an optical signal is coupled to a multimode optical fiber (figure 3, col. 3 lines 32-58) and the means for equalizing comprises means for equalizing multimode dispersion from the multimode optical fiber (Abstract).

For claims 38-42, Azadet et al. do not expressly disclose wherein the means for receiving an optical signal is coupled to a single mode optical fiber and the means for equalizing comprising means for equalizing chromatic and/or waveguide dispersion from the single mode optical fiber. Winter et al disclose wherein the means for receiving an optical signal is coupled to a single mode optical fiber (figure 1, page 305.3.1, col. 2 line 12) and the means for equalizing comprising means for equalizing chromatic and/or waveguide dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29).

Azadet et al. disclose is coupled to a multimode optical fiber (figure 3, col. 3 lines 32-58) and Winter et al. in view of Azadet et al. disclose wherein the means for receiving an optical signal (figure 1, page 305.3.1, col. 2 line 12) and the means for equalizing comprises means for equalizing chromatic and/or waveguide dispersion in the multimode optical fiber (figure 7, page 305.3.6 col. 1 lines 28-29 as set forth in claim 39); Azadet et al. disclose is coupled to a multimode optical fiber (figure 3, col. 3 lines 32-58) and Winter et al. in view of Azadet et al. disclose wherein the means for receiving an optical signal (figure 1, page 305.3.1, col. 2 line 12) and the means for equalizing comprises means for equalizing comprises means for equalizing polarization mode dispersion from the single mode optical fiber (figure 7, page 305.3.6 col. 2 lines 28-31 as set forth in claim 40); wherein the means for receiving an optical data signal is coupled to a single mode optical fiber (figure 1, page 305.3.1 col. 2 line 12) and the means for equalizing comprises means for equalizing dispersion induced in the single mode optical fiber by laser chirping (page 305.3.2, col. 2 lines 10-14 as set forth in claim

41); wherein the means for receiving the optical data signal from a transmitter that lacks external modulators (figure 1, page 305.3.1, col. 2 lines 3-5 and col. 2 line 12), and the means for equalizing comprises means for equalizing excess dispersion induced by laser chirping (page 305.3.2, col. 2 lines 10-14 as set forth in claim 42).

One skilled in the art would have recognized the means for receiving the optical data signal from a single mode optical fiber to use the teachings of Winter et al. in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use receiving the optical data signal from a single mode optical fiber as taught by Winter et al. in Azadet et al.'s system with the motivation being to convert the optical signal, $s_0(t)$, to an electrical signal (page 305.3.1 lines 12-14).

6. Claims 43-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Azadet et al. (EP 1006697) in view of Winter et al. (Electrical Signal Processing Techniques In Long-Haul, Fiber-Optic Systems, AT&T Bell Laboratories) further in view of John A.C. Bingham (Multicarrier Modulation for Data Transmission: An Idea Whose Time Has Come, IEEE Communication Magazine, May 1990).

For claims 43-51, Azadet et al. in view of Winter et al do not expressly disclose wherein step (5) comprises decoding a convolutional code. In an analogous art, John A.C. Bingham discloses wherein step (5) comprises decoding a convolutional code (page 12, col. 2 lines 42-45).

John A.C. Bingham discloses wherein step (5) comprises decoding a trellis code (page 12, col. 2 line 14 as set forth in claim 44); wherein step (5) comprises decoding a

block code (page 12, col. 2 lines 43-45 as set forth in claim 45); wherein the digital signals processor comprises a convolutional decoder (page 12, col. 2 lines 42-45 as set forth in claim 46); wherein the digital signals processor comprises a trellis decoder (page 12, col. 2 line 14 as set forth in claim 47); wherein the digital signals processor comprises a block decoder (page 12, col. 2 lines 42-45 as set forth in claim 48); wherein the means for performing digital process on the samples comprises means for decoding a convolutional code (page 12, col. 2 lines 42-45 as set forth in claim 49); wherein the means for performing digital processes on the samples comprises means for decoding a trellis code (page 12, col. 2 line 14 as set forth in claim 50); wherein the means for digitally performing digital processes on the samples comprises means for decoding a block decoder (page 12, col. 2 lines 42-45 as set forth in claim 51).

One skilled in the art would have recognized decoding a convolutional code to use the teachings of John A.C. Bingham in the system of Azadet et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use the decoding a convolutional code as taught by John A.C. Bingham in Azadet et al.'s system with the motivation being desired that all of the data on one symbol (block) be decoded in the same period and from only the signals received within that block (page 12, col. 2 lines 43-45).

Response to Arguments

7. Applicant's arguments filed 05/08/06 have been fully considered but they are not persuasive.

The applicant argues with respect to claims 1, 9, and 18, that neither Azadel nor Winters, alone or in combination, teach or suggest M parallel digital processing paths and N ADC paths, wherein M≠N, as recited in independent claims 1, 9 and 18. The examiner disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., M≠N) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, there is no support could be found in the original specification for this feature limitation "1/s, where s is an integer greater than one". Therefore, it is believed that the rejections should be sustained.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D. Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TN
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